

**FIG. 1**

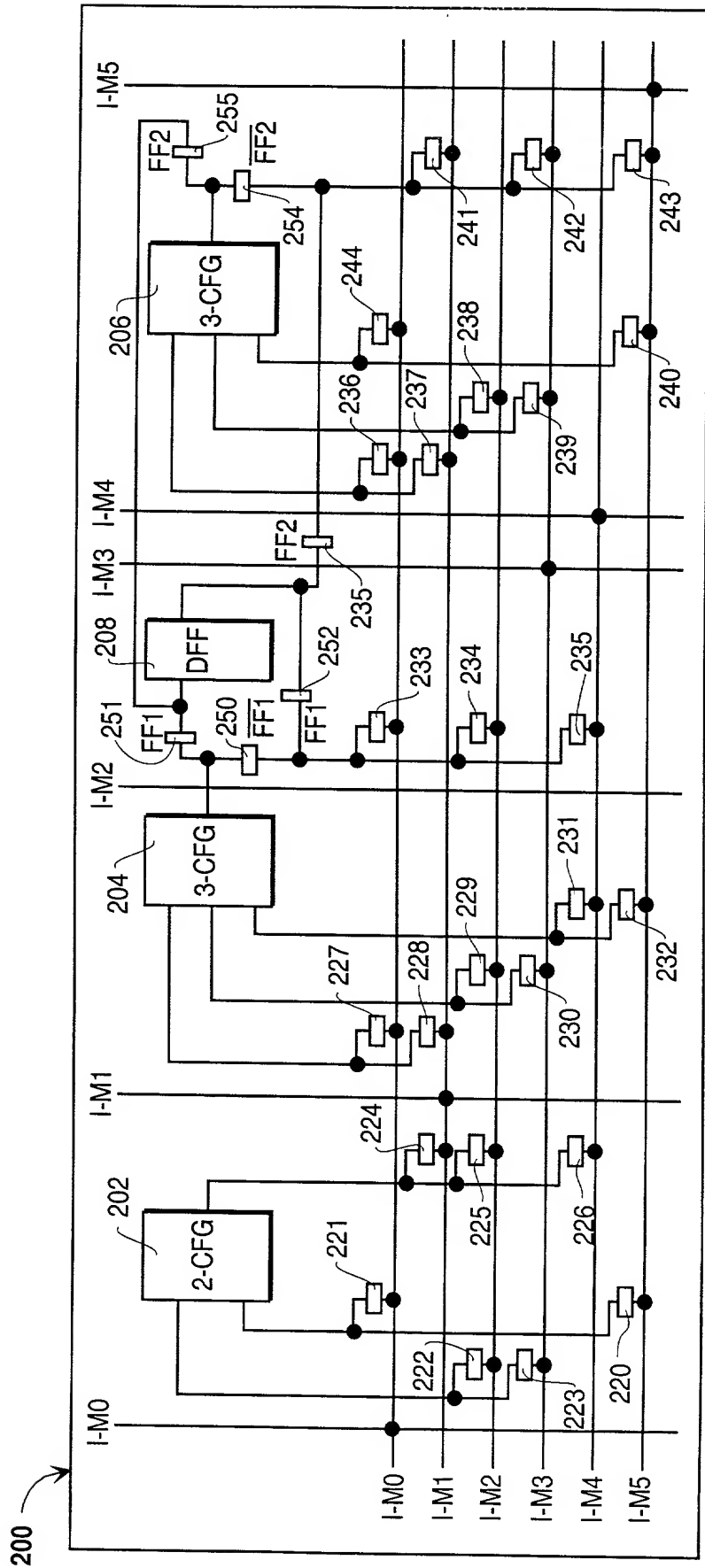


FIG. 2A

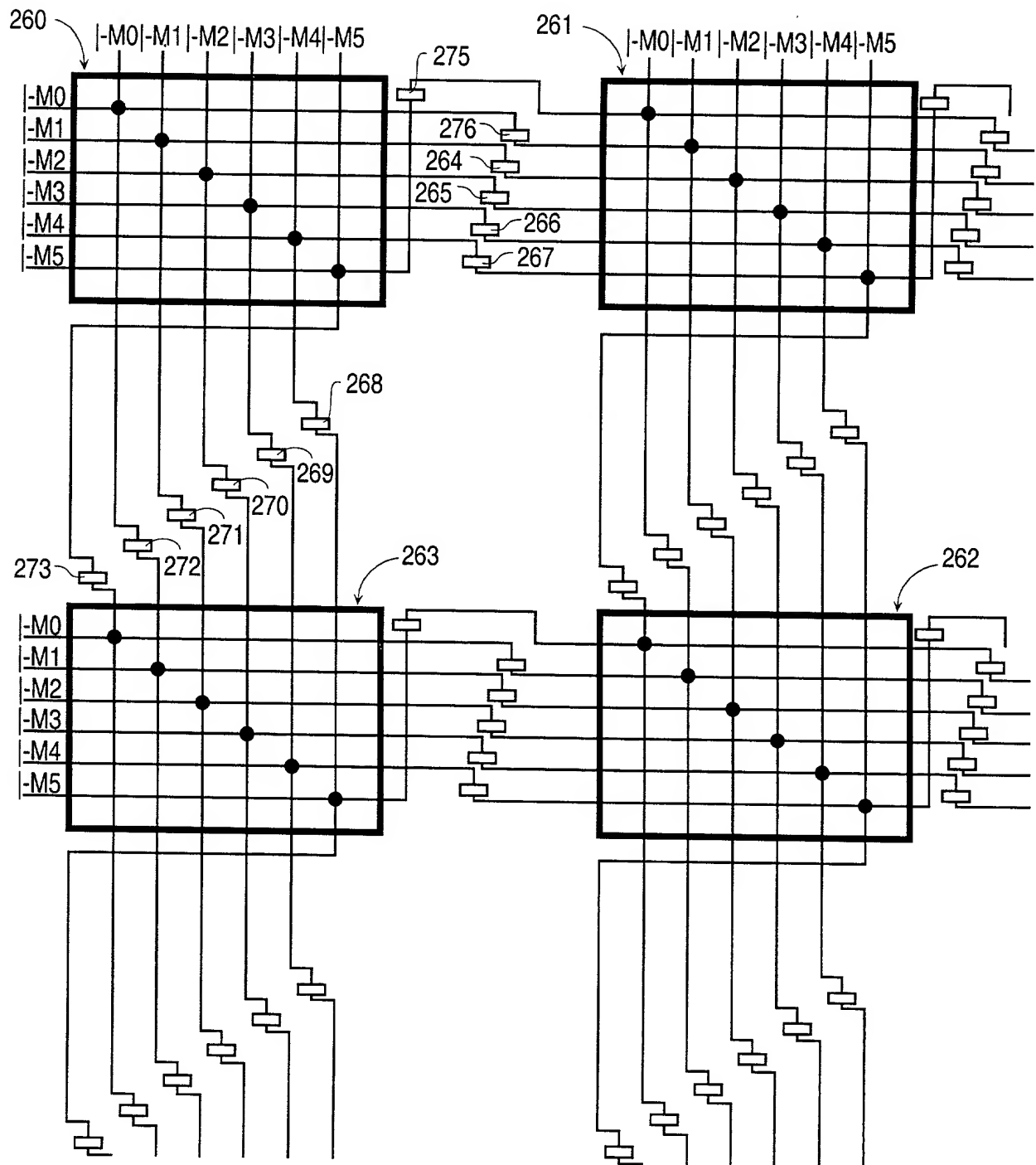
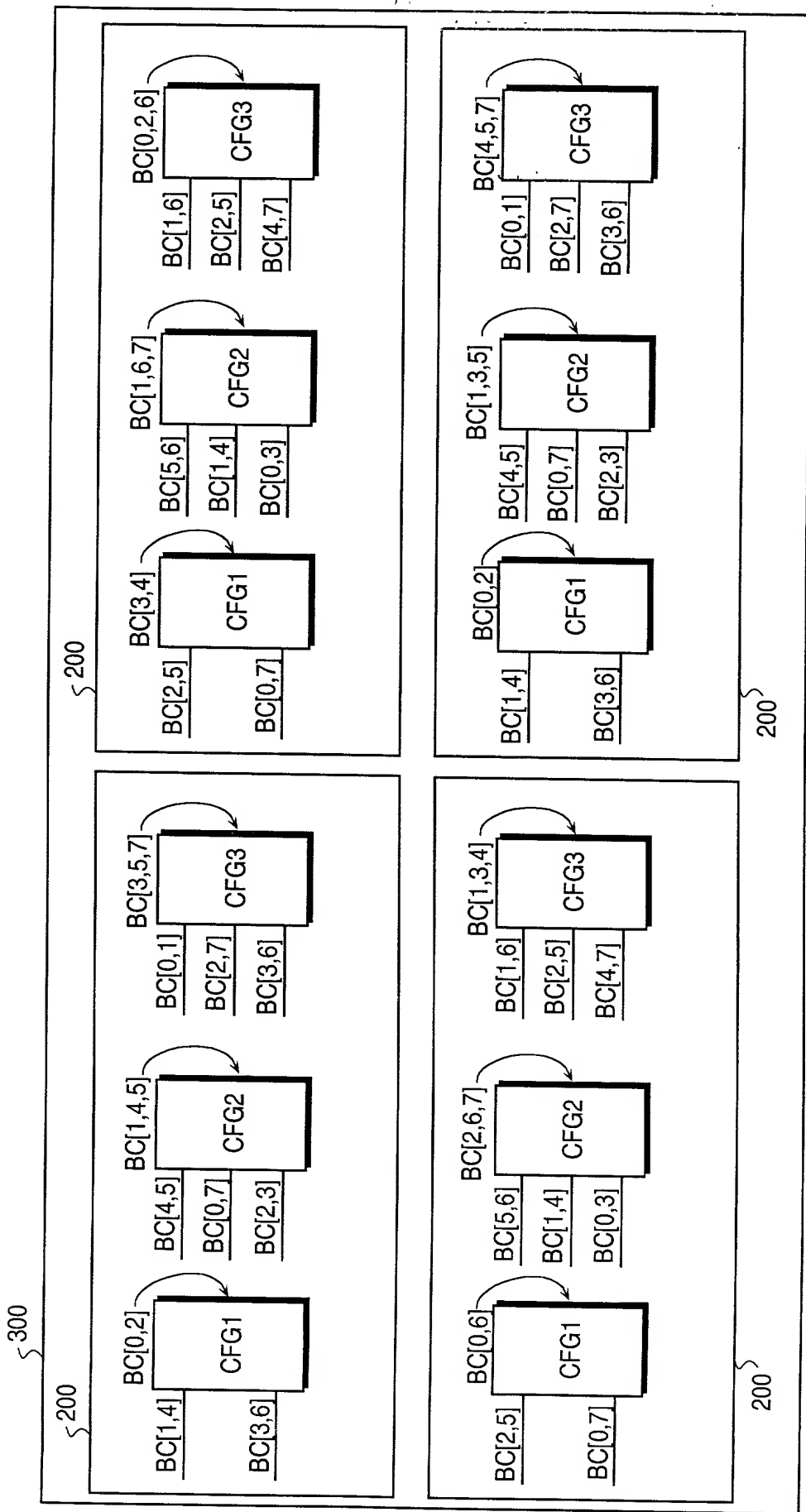
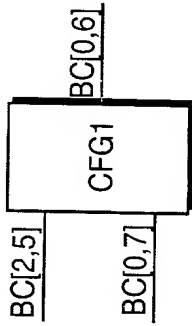


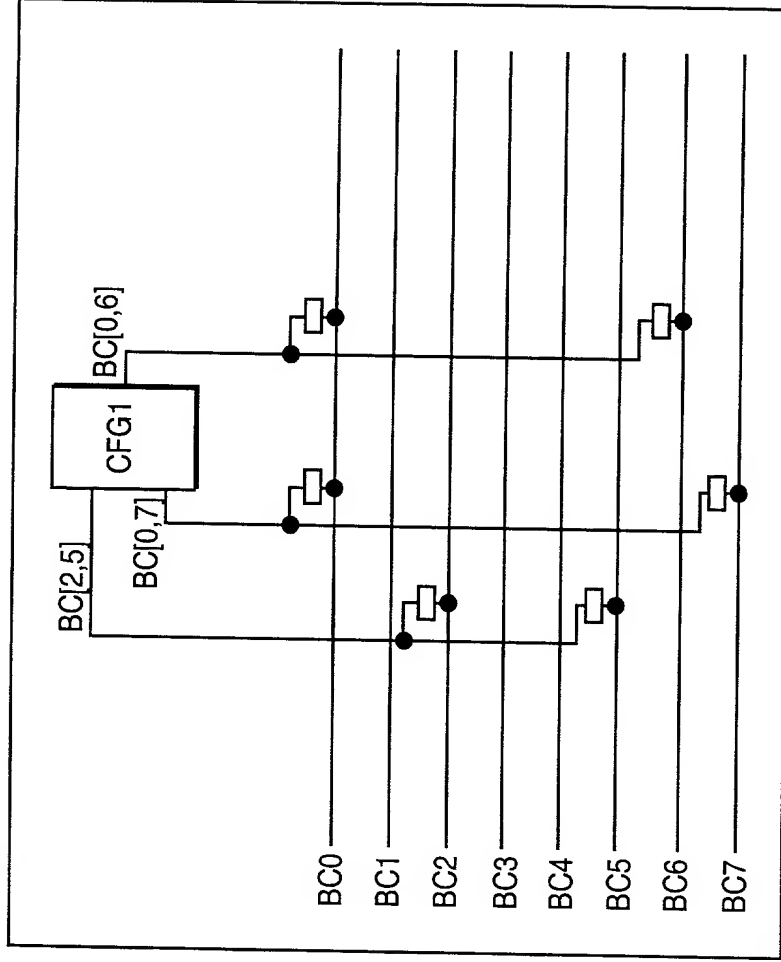
FIG. 2B



**FIG. 3A**

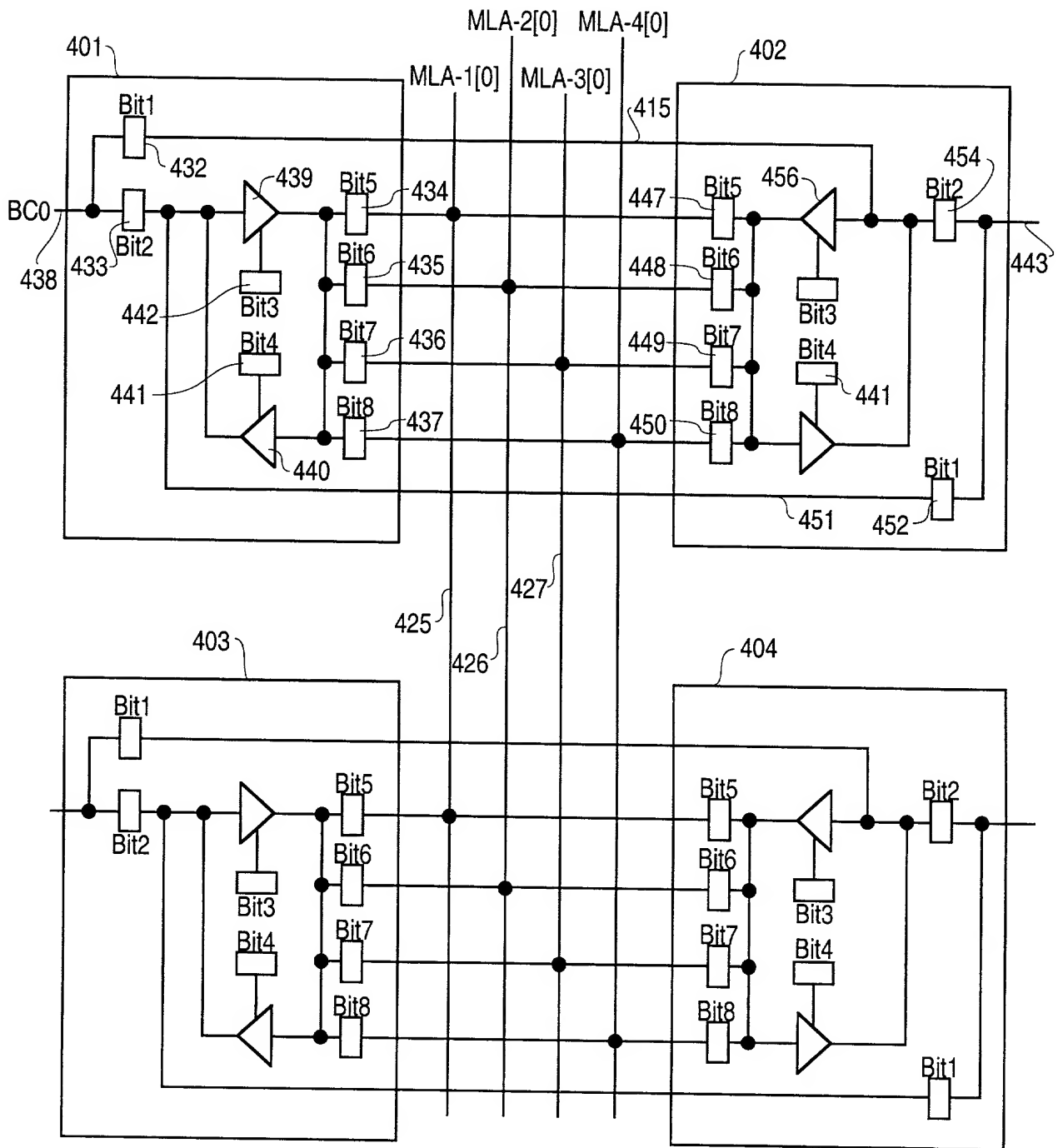


**EQUALS**



**FIG. 3B**





**FIG. 4B**

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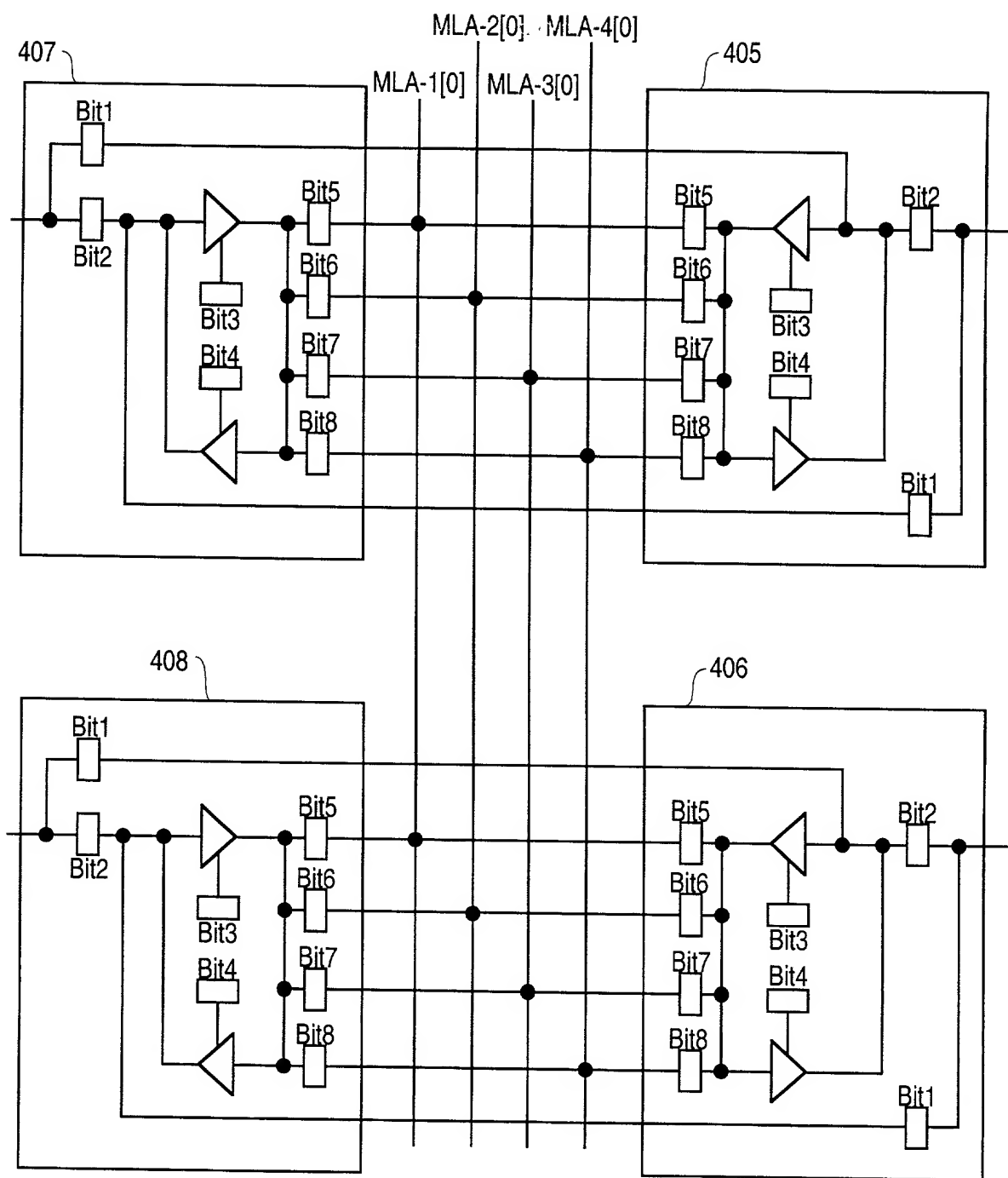
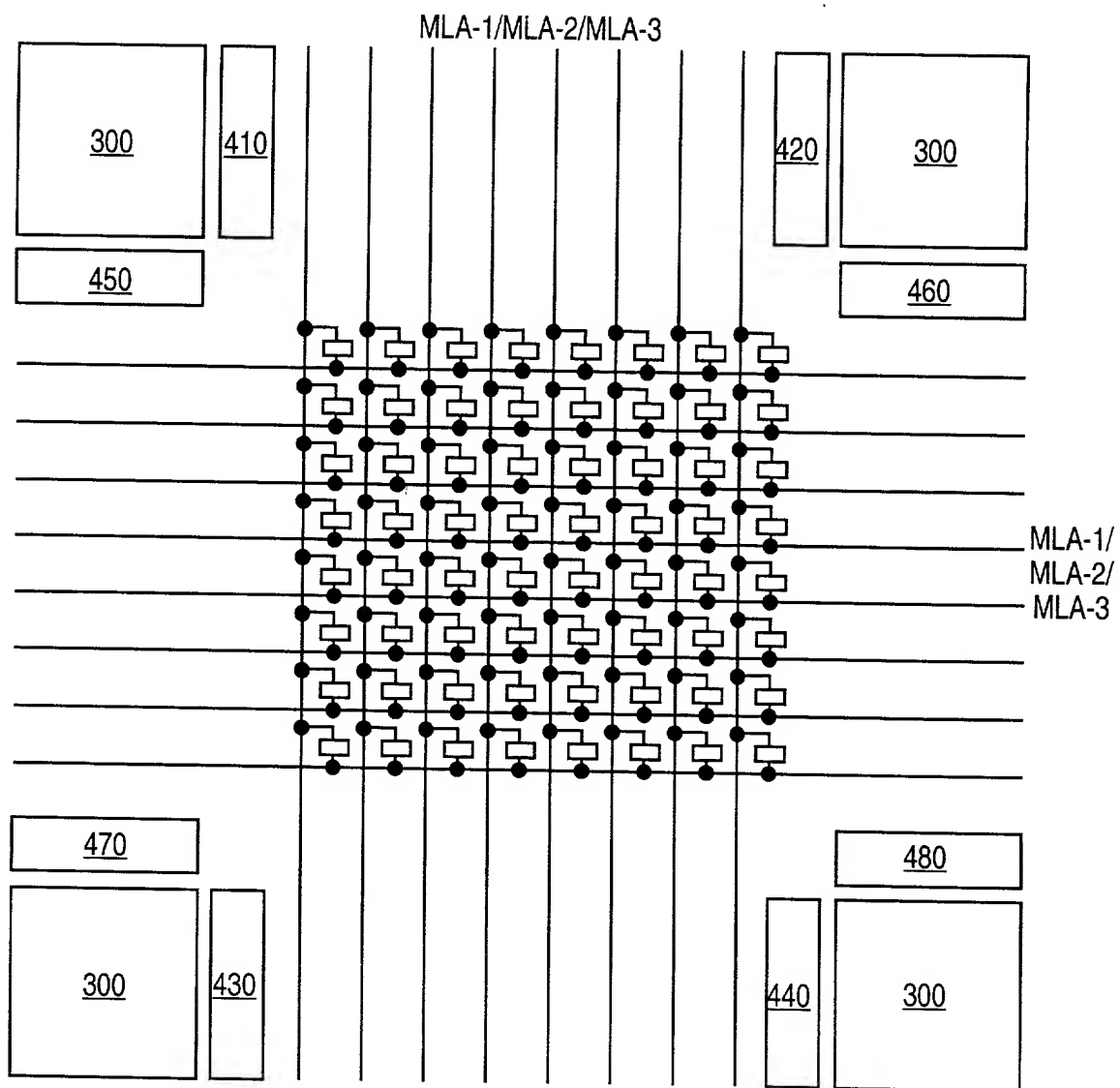
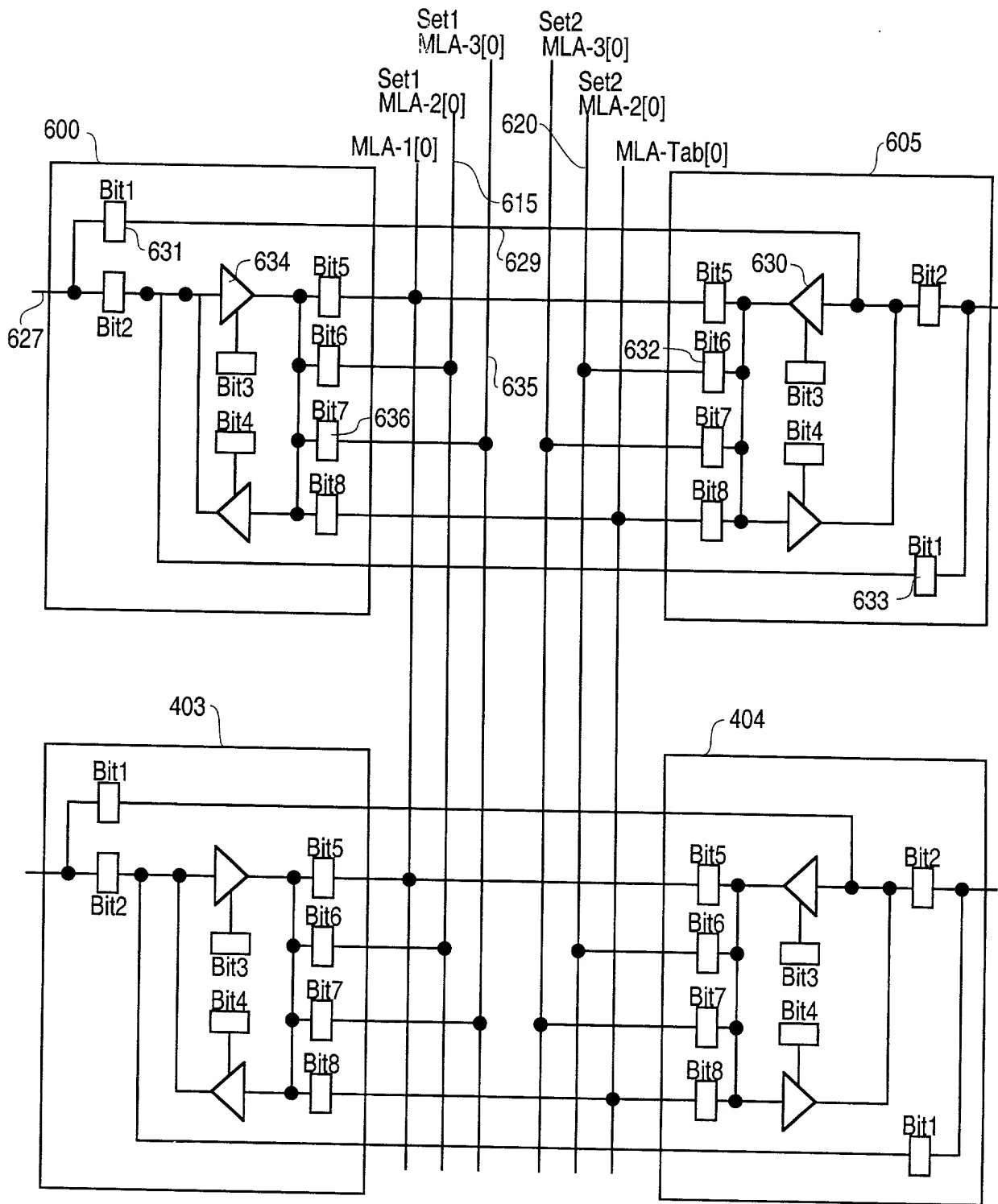


FIG. 4C

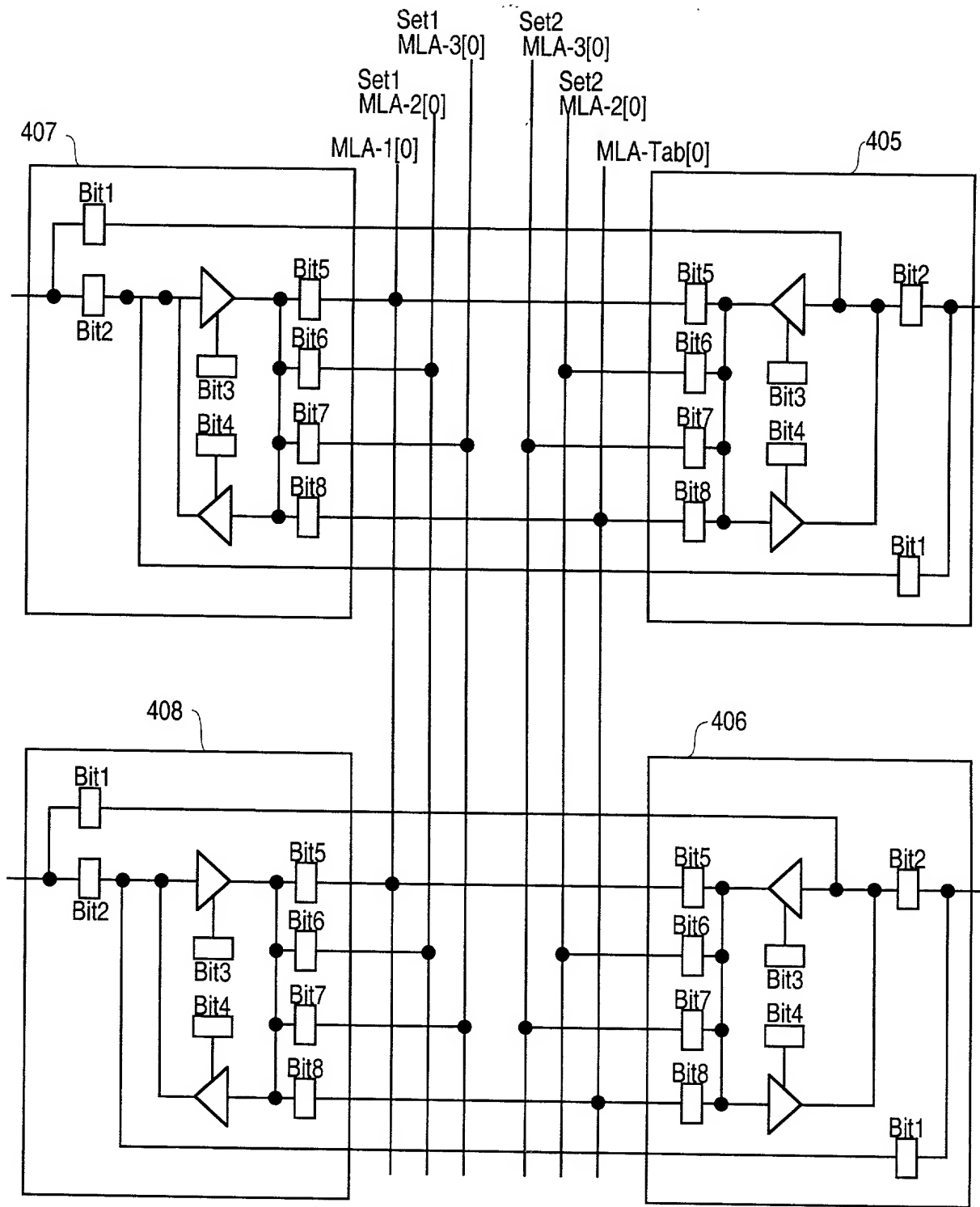




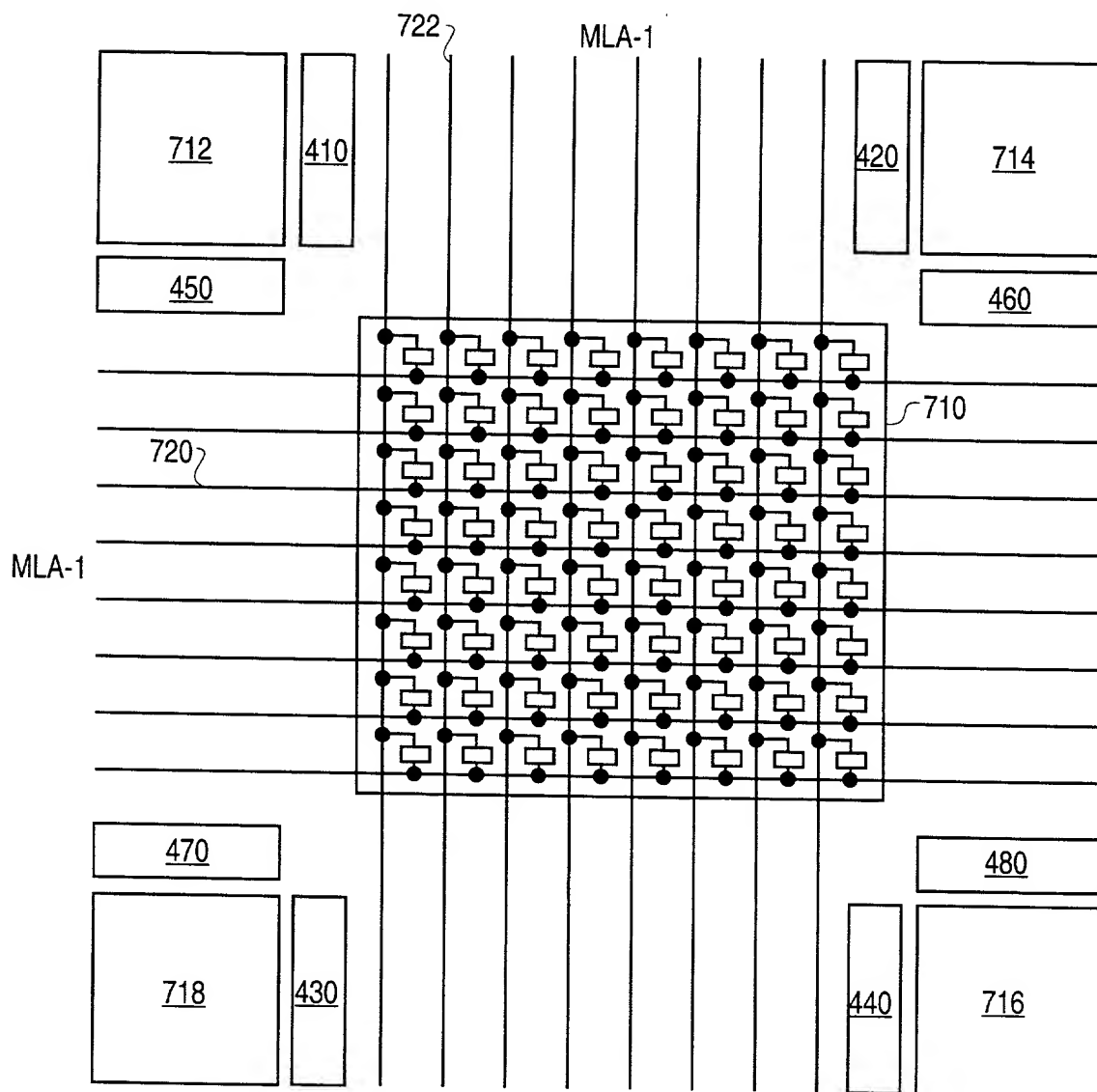
**FIG. 5**



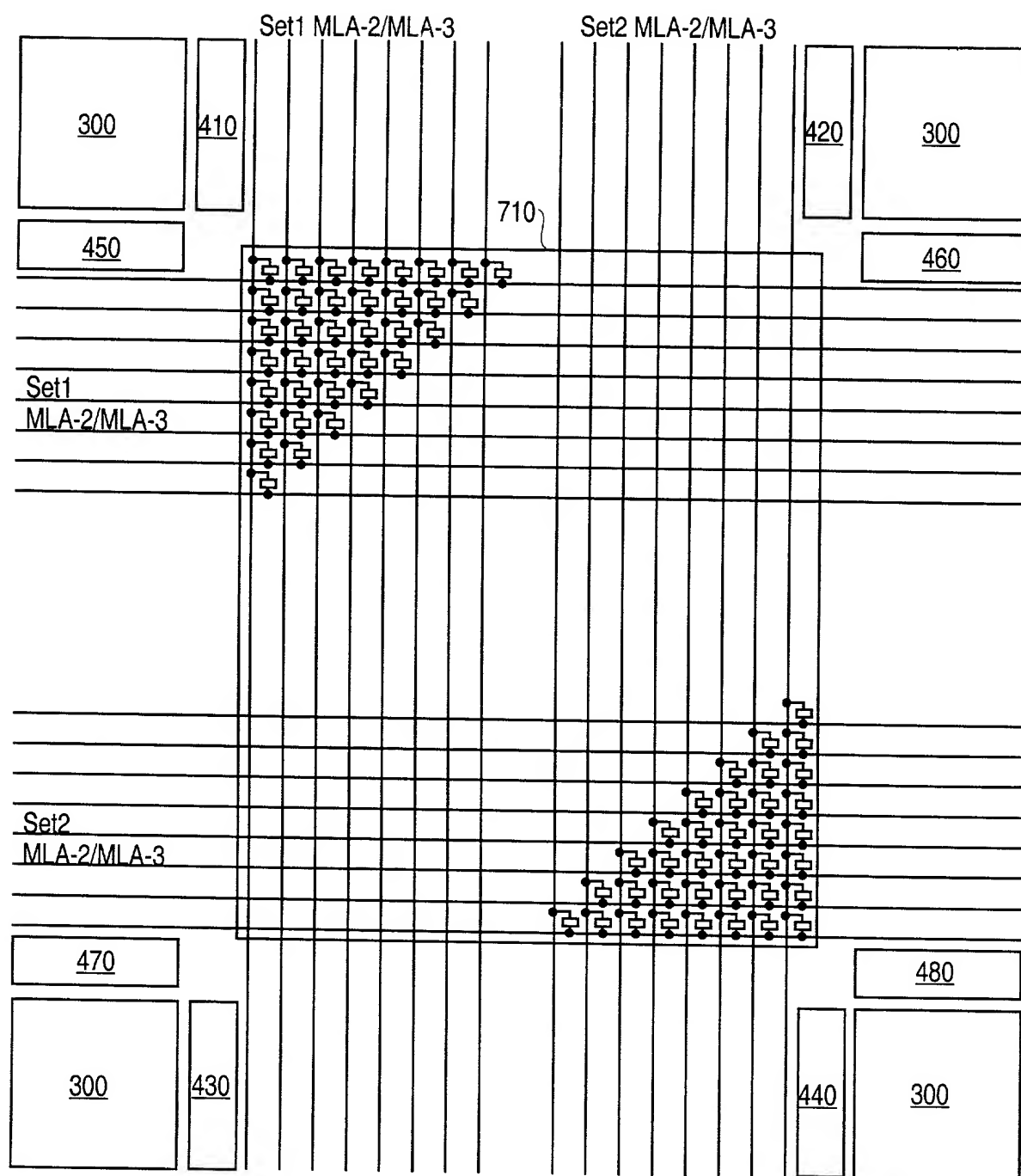
**FIG. 6A**



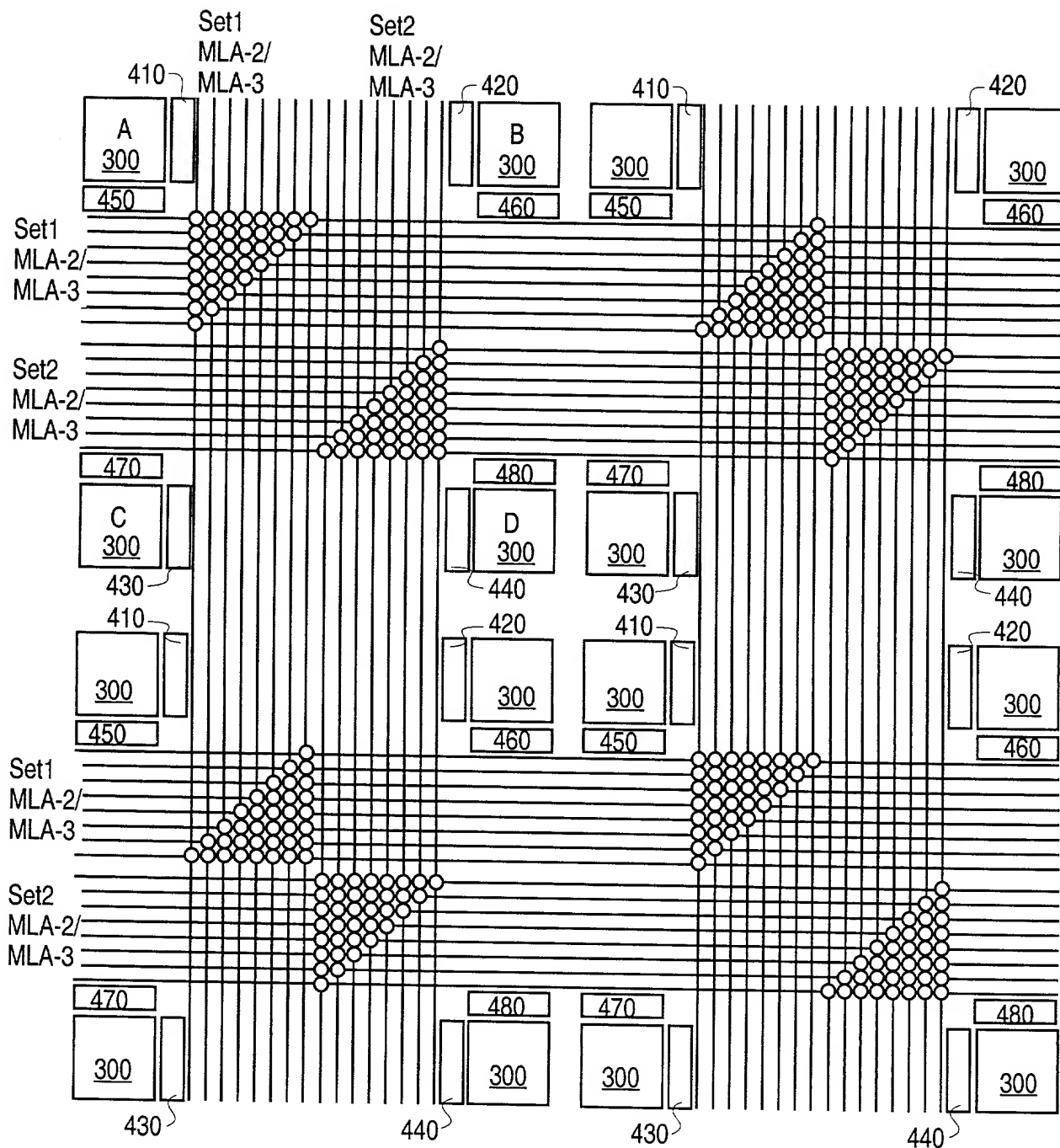
**FIG. 6B**



**FIG. 7A**



**FIG. 7B**



**FIG. 7C**

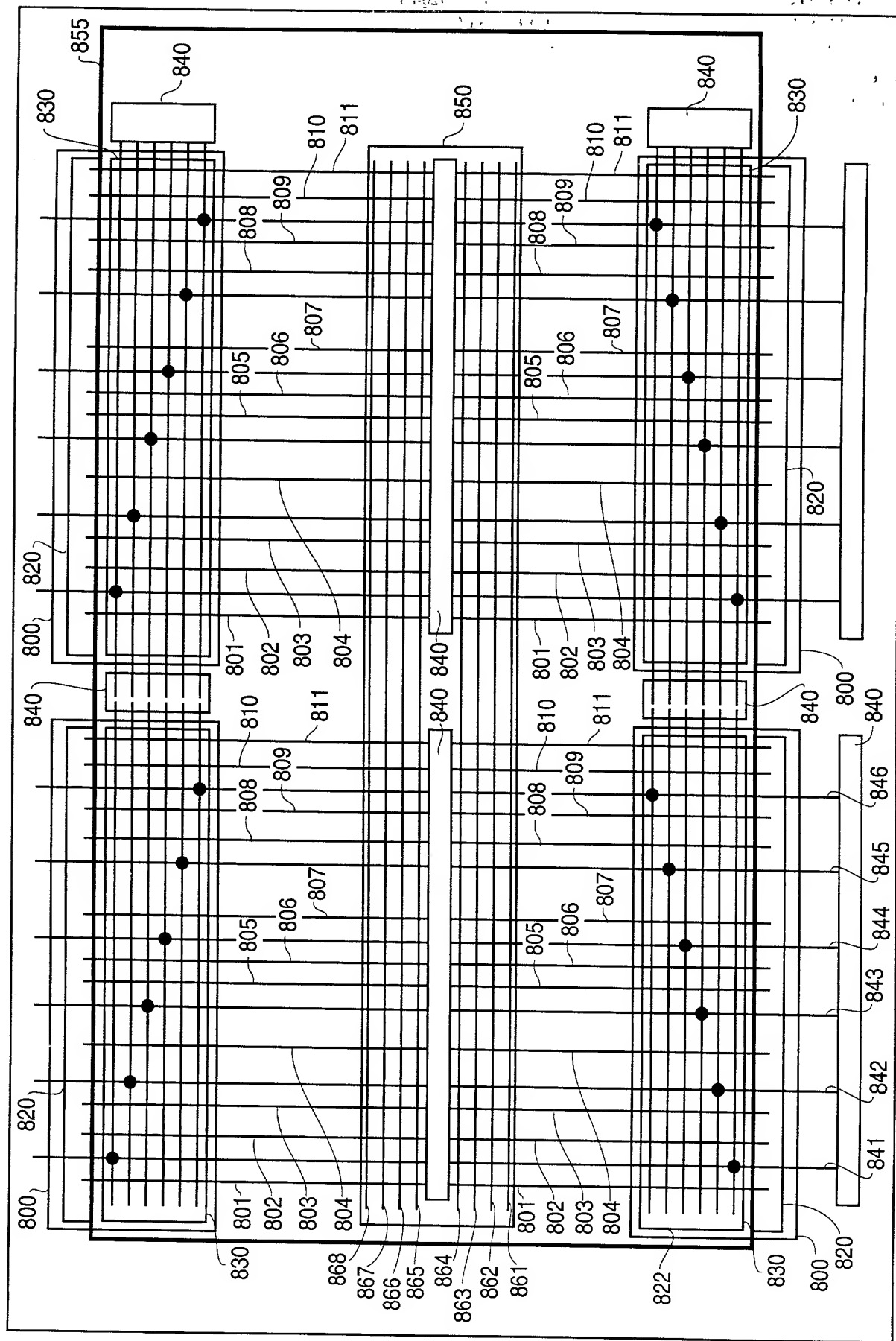
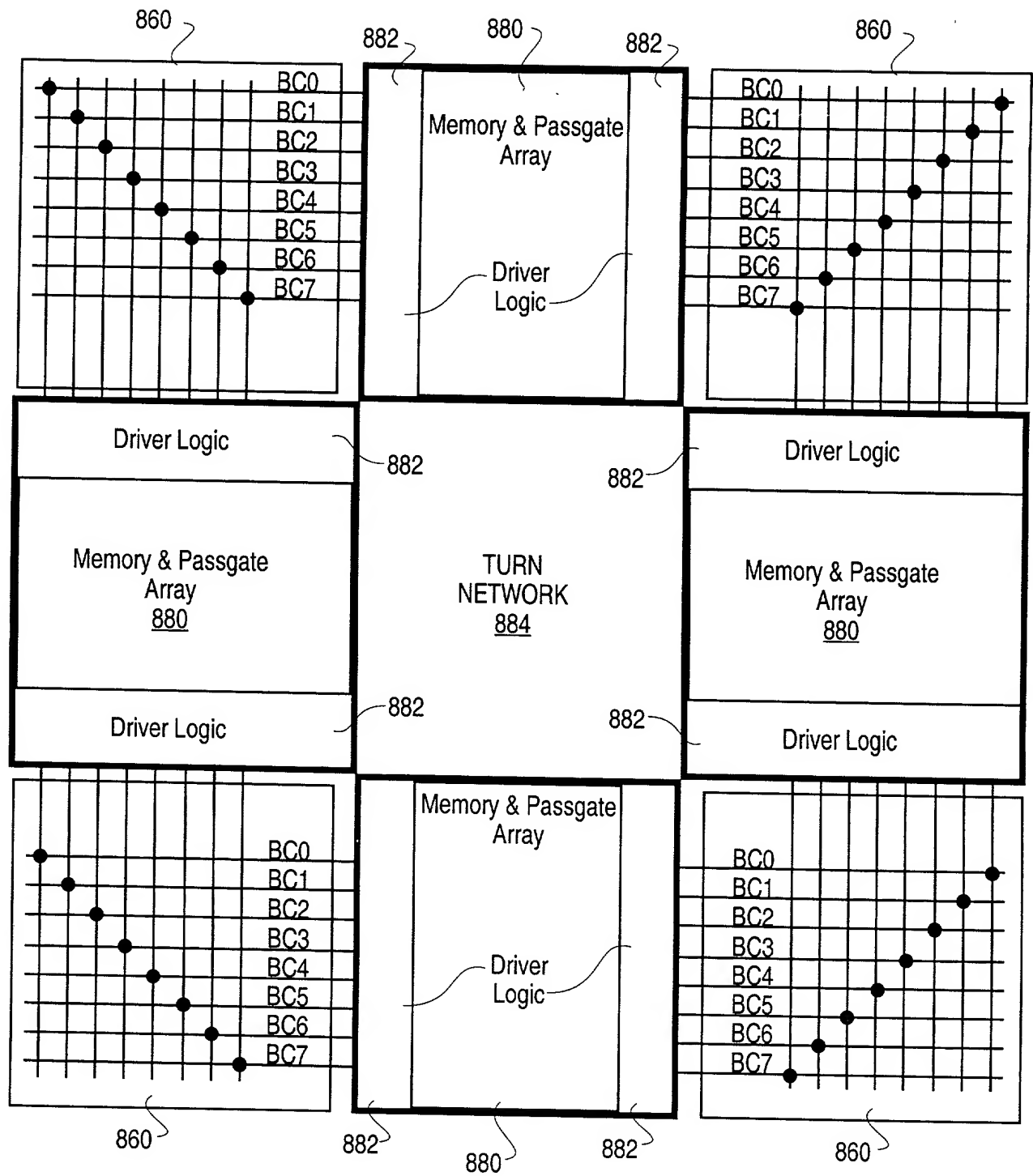
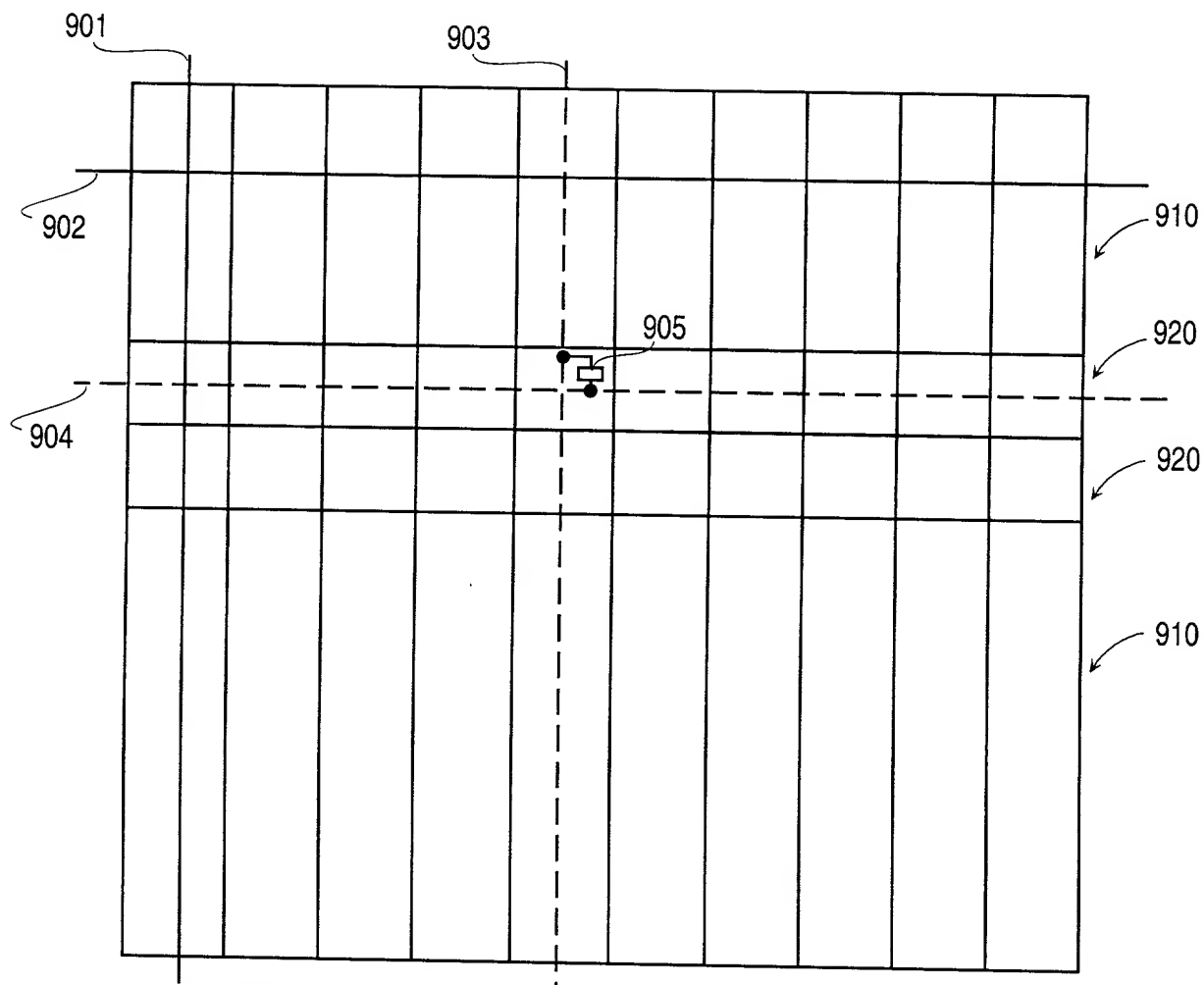


FIG. 8A



**FIG. 8B**





910 : MEMORY BITS  
 920 : PASSGATES  
 901, 902 : ADDRESSING LINES x - y  
 903, 904 : ROUTING LINES  
 905 : PROGRAM CONTROLLED PASSGATE BETWEEN 903 AND 904

**FIG. 9** EXAMPLE OF CONTIGUOUS MEMORY AND PASSGATE ARRAY LAYOUT ORGANIZATION